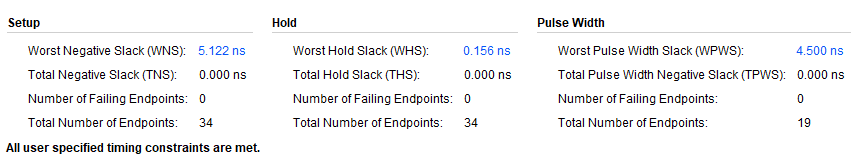
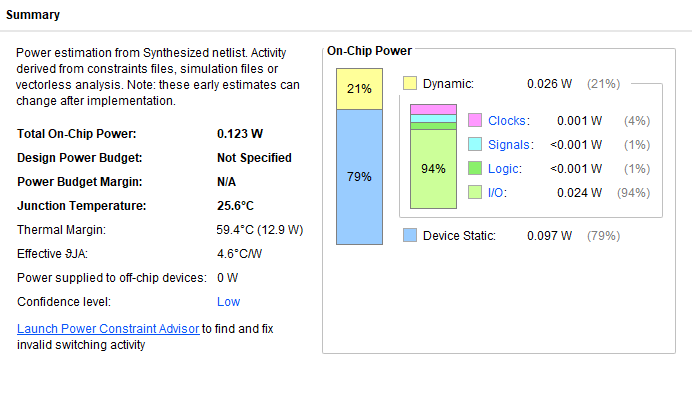
Synthesis stage:

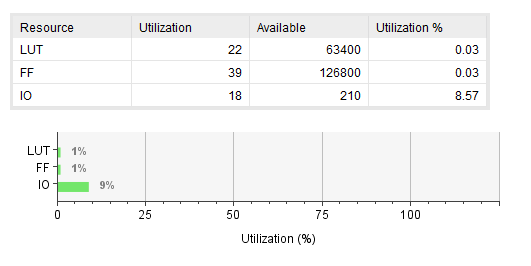
* STA:



* Power Analysis:

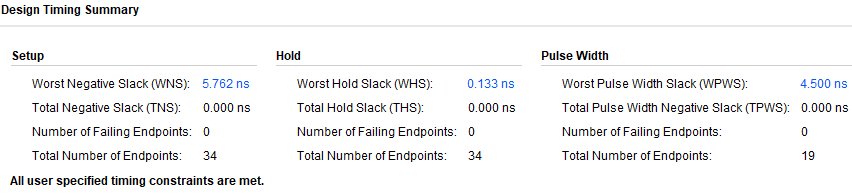


* Utilization Report:

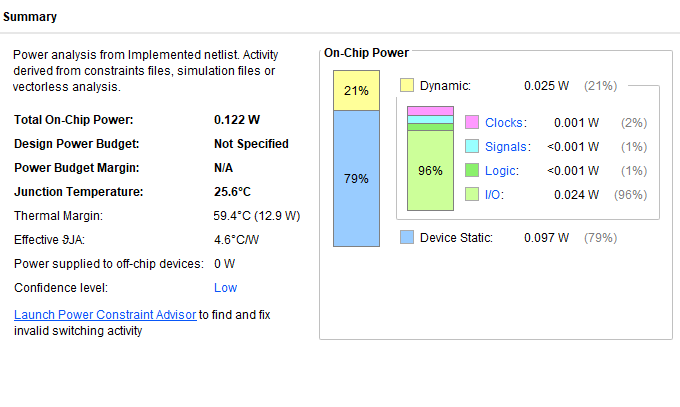


Implementation:

* STA:



* Power Analysis:



* Utilization Report:

